ELECTRONICS PARTS SER CUSTOMIZED SOCKETS & CONNECTORS 株式会社 エス・イー・アール

ARDENT CONCEPTS

Application Note

#105 – April 2016

TR Multicoax Series Board Optimization Procedure

Purpose: This application note provides detailed information on how printed circuit boards can be optimized for TR Multicoax series use.

OPTIMIZATION PROCEDURE

- The optimization checklist provides the input parameters for simulating the unique information stack up of every board. This must be filled out prior to beginning any optimization work.
- For the TR assembly there is an optional optimization report that determines footprint specification parameters for improved impedance matching.
- The default optimization return loss performance for the TR assembly at the connector is -20 dB for up to 20 GHz and -12 dB from 20 GHz to 40 GHz.
- The current footprint for the connector has tolerance limitations for modifications.

HFSS SIMULATION

The simulation determines the optimal board footprint parameters for TR. The simulation models the performance of a signal as it transitions under the connector, thru the interface, and up to a few inches of coax cable.

- The default optimization return loss performance for the TR assembly at the connector is -20 dB for up to 20 GHz and -12 dB from 20 GHz to 40 GHz.
- The current footprint for the connector has tolerance limitations for modifications.

The parameters kept constant for simulation optimizations are the following:

- Gap width under the connector.
- Anti-pad ground diameter and microstrip top metal return channel width (guard channel).
- Via diameter
- Return via bolt circle diameter

- Return via location on the bolt circle

The parameters frequently adjusted during the optimization phase are the following:

- Signal capture pad diameter
- First return layer anti-pad diameter
- Trace width under connector

See Figure 17 for the tuned footprint simulation parameters.

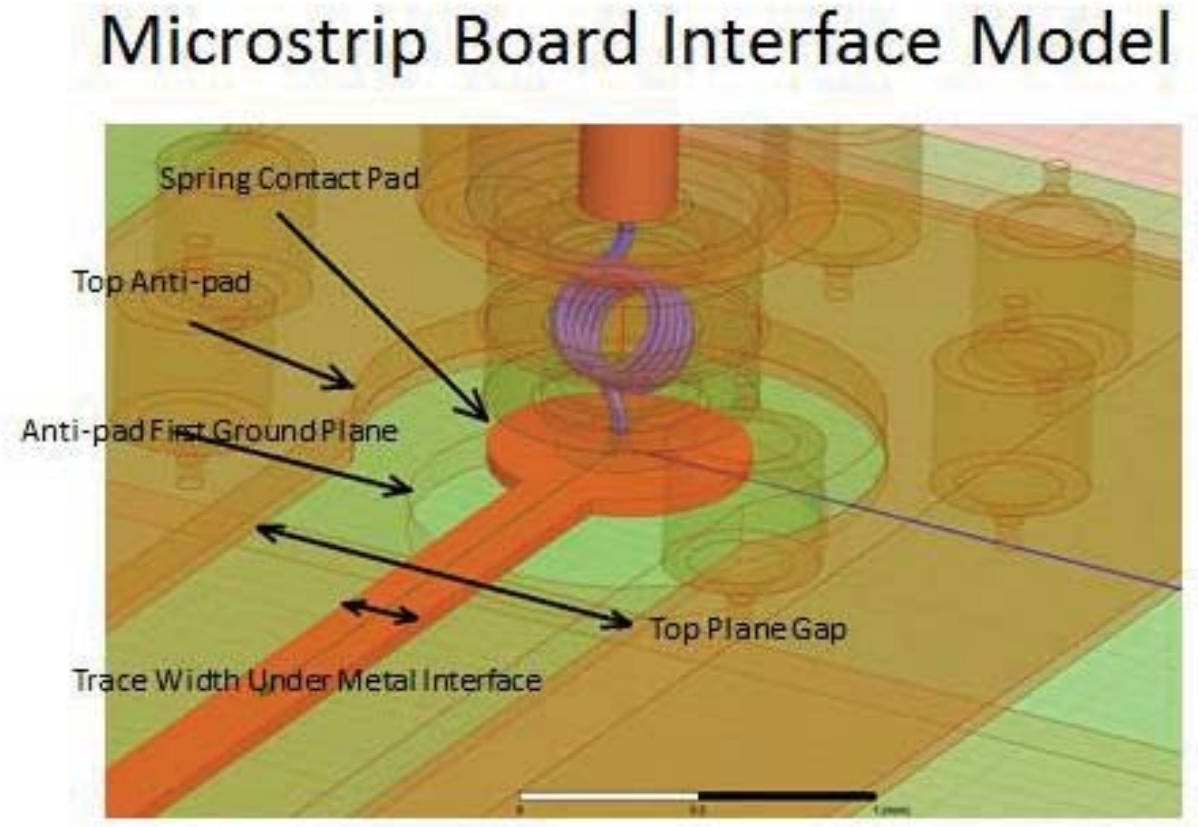

Figure 17: Tuned Simulation Parameters

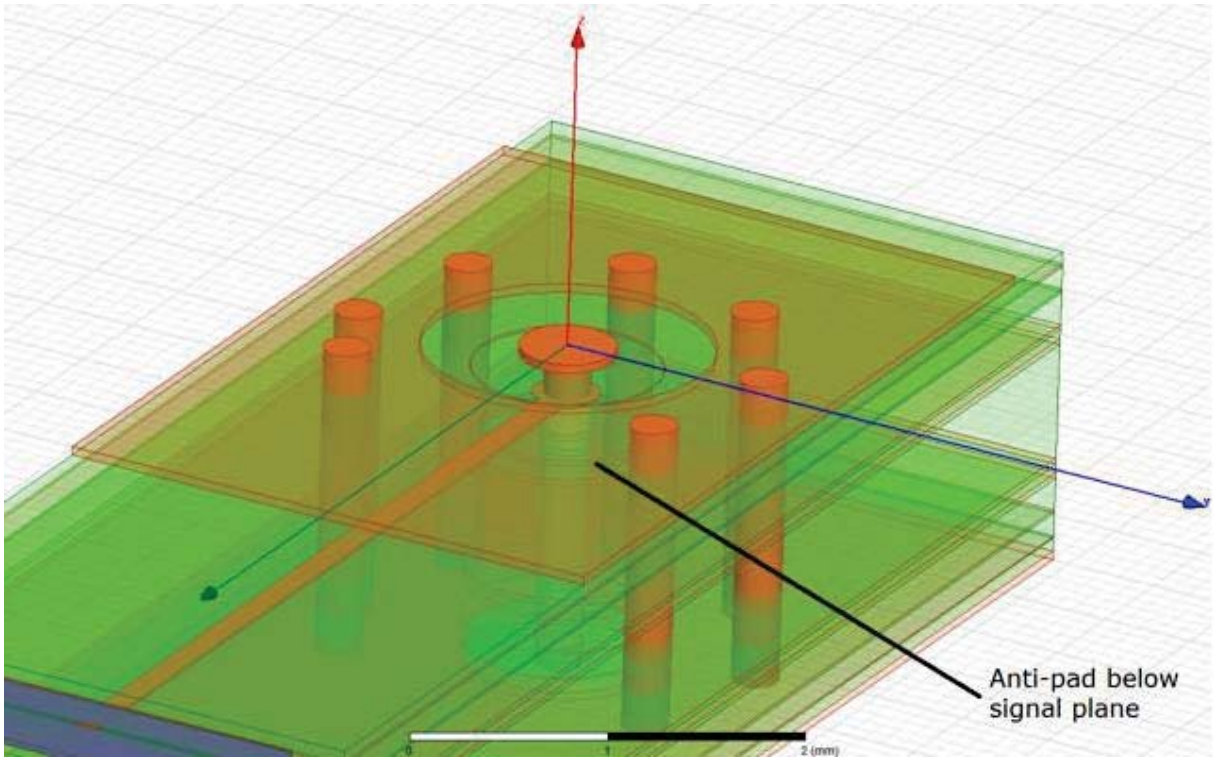

Figure 18: Stripline Model Showing the Through 83 mil Diameter Ground Via Bolt Circle Coax Structure

OPTIMIZATION REVIEW

After the variable parameters have been quantified, a report is compiled that provides the new connector footprint parameters.

Thru Scattering parameter graphs are provided to quantify the reflected and transmitted power with the new footprint optimization parameters.

The following simulated S-Parameter graphs are provided:

Return Loss, Insertion Loss, Step Response Time Domain Reflection (TDR)

NOTE: The current footprint for the connector has tolerance limitations for modifications.
The Time Domain Reflection graph provides a high resolution image of impedance values with a rise time of 25 ps for a frequency span bandwidth of 40 GHz.

NOTE: The graphs provide a forward and reverse pathway thru the connector (legend indicated by coax and microstrip), (See Figures 19-21).

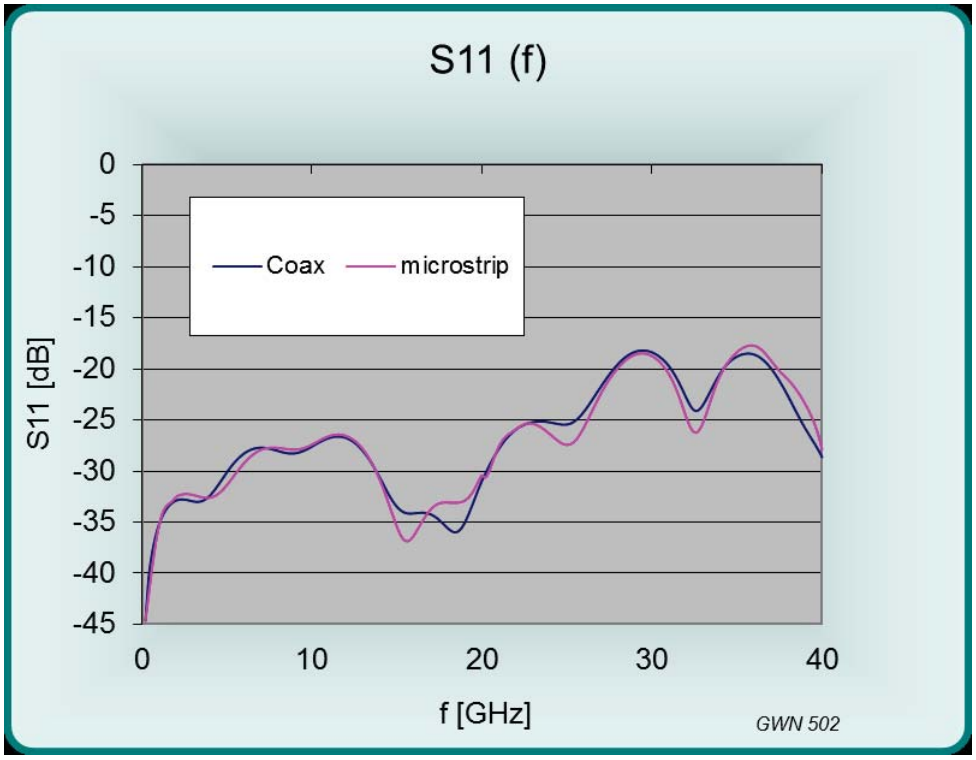

Figure 19: Optimized Return Loss Simulation

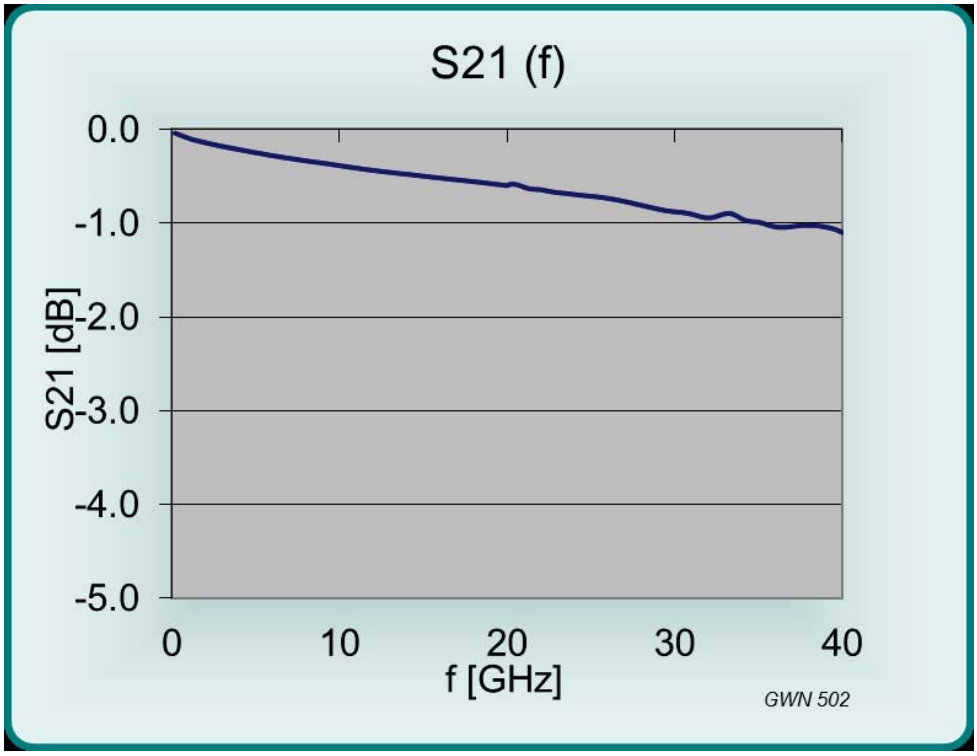

Figure 20: Optimized Insertion Loss Simulation

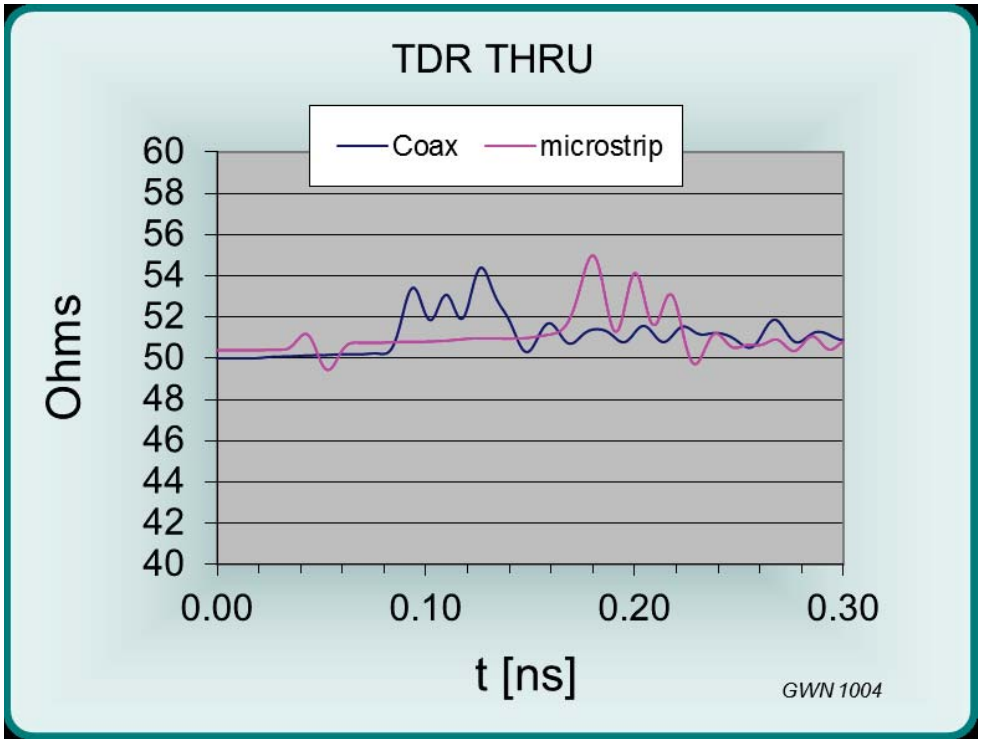

Figure 21: Optimized Time Domain Reflection Simulation (Step Response Rise Time: 10 ps)
Note: Standard is 25 ps

NARROW TRACE TRANSITION UNDER TR ASSEMBLY

Since there is a grounded metal air gap channel under the connector, a capacitive reaction will occur and a narrower inductive trace is required under the connector.

A model of the interface is included in the simulation and the channel height is 4.5 mils.

The HFSS simulation models the narrow trace transition with approximately 0.5 inches of the incident board trace.

FINAL BOARD REVIEW

After the board optimization parameters have been verified and implemented, a new board file is sent to Ardent Engineering to verify that TR will be compatible with your board.
Procedure Includes:

Verification of Footprint Specification Tolerances with Cadence Board File Viewer

NOTE: The final board review does not contain HFSS model, only simulation results. A model may be attainable. Please consult factory here.

After the board file has been reviewed, specifications or configurations measured out of tolerance are noted and corrections are recommended.

Approval of a board footprint is awarded when specifications are determined within tolerance.

The final board review will also communicate reminders of important parameters to consider.

IMPORTANT NOTE

Verify Board Integration:

- Filled Contact Vias
- No Soldermask Area under Connector
- No Narrow Trace Width Tapers

REFERENCE MATERIALS

OPTIMIZATION COMPARISON CHART

The Optimization Chart compares results of optimization simulations and corresponding parameter changes.

Microstrip Parameter	Example 1 (mils)	Example 2 (mils)	Example 3 (mils)	Example 4 (mils)	Evaluation Board (mils)	Footprint (mils)
Connector Contact Pad Diameter	17.8	17.8	17.8	17.8	17.8	20
Top Trace Width Underneath Connector Body	10.6	9.1	8.5	10.2	10.6	6.0
Gap Width on Top Plane	50	50	50	50	50	50
Anti-pad Diameter on Top Plane	60.3	60.3	60.3	60.3	60.3	60
Anti-pad Diameter in GND Plane Below Trace	55.9	56.7	43.3	51.2	51.2	40.2
Extension of Narrow Trace Outside connector body	0	0	0	0	0	0
Dielectric Thickness	10.0	8.7	5.0	5.5	10.0	4.7
Dielectric Type First Layer	Rogers 4350	Rogers 4003	Rogers 3003	Nelco SI	Rogers 3003 (ENIG)	Megtron 6 (HVLP)
Dielectric Constant	3.48	3.38	3.1	3.4	3.1	3.6

Application Note Summary

- Optimization checklist must be filled out prior to beginning any optimization work.
- Optional optimization report that determines footprint specification parameters.
- Default optimization return loss performance for the TR assembly at the connector is -20 dB for up to 20 GHz and -12 dB from 20 GHz to 40 GHz.
- The following simulated S-Parameter graphs are provided with optimization:
    - Return Loss, Insertion Loss, Step Response Time Domain Reflection (TDR)
- Since there is a grounded metal air gap channel under the connector, a capacitive reaction will occur and a narrower inductive trace is required under the connector.
- The final board review does not contain HFSS model, only simulation results. A model may be attainable. Please consult factory here.

END OF DOCUMENT

Who is Ardent Concepts

Ardent Concepts, Inc. is a leading designer and manufacturer of high performance multicoax, probes, connectors, sockets used in the development of next generation semiconductors and electronics systems. Our core technology is the smallest, fastest, most electrically efficient compression mount connector technology worldwide. It is used to connect: integrated circuits and printed circuit boards to instrumentation and to each other offering superior signal integrity in a high speed environment. Markets for our products include: Semiconductor, Test & Measurement, Military/Aerospace, Communications and Medical.

Contact Information:

Phone: (603) 474-1760
E-mail: info@ardentconcepts.com
Ardent Concepts
130 Ledge Road
Seabrook, NH 03874

Sales:
sales@ardentconcepts.com

Technical:
engineering@ardentconcepts.com